LV8726TA

Advance Information

ON Semiconductor®

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Bi-CDMOS IC

PWM Constant-Current Control Stepper Motor Pre-Driver

Overview

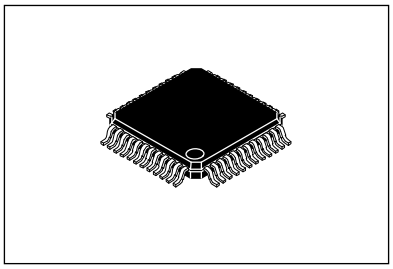
LV8726TA is a stepper motor pre-driver for a bipolar stepper motor that can drive PWM constant current control and uses external P-N channel MOSFETs. The device integrates sixteen step modes from half step to 1/128 step and suits for various industrial equipment.

The operation voltage is high at 9V to 55V, and a motor can easily drive by CLK input.

Operation of a device can be programed by a SPI serial interface.

Step mode, output current ratio, decay mode, blanking time and chopping(PWM) period are programmable via a SPI serial interface.

The device can reduce current consumption by setting standby mode, when idle.



TQFP48 EP 7×7 , 0.5P

Feature

- 1 channel PWM constant-current control stepper motor pre driver of P-N channel MOSFET drive
- BiCDMOS process IC
- 1/2,1/4,1/8,1/16,1/32,1/64,1/128 Step and, 1/3,1/6,1/12,1/36,1/5,1/10,1/20,1/50,1/100 Step are selectable.
- Advance the excitation step with the only step signal input
- 8-bit 3-wire serial control
- Over-current protection circuit
- Low voltage protection circuit
- Thermal shutdown circuit
- Input pull down resistance
- With reset pin and enable pin

Typical Applications

- Textile machine
- Packing machine
- Large printer
- Engraving machine
- Industrial instrument

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 34 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	VM max	VM	60	V
Output current	I_O max	GU1,GU2,GU3,GU4 GB1,GB2,GB3,GB4	50	mA
Logic supply voltage	VCCmax	VCC	6	V
Logic input voltage	V_{IN} max	ST,SCLK,SDATA,STB,STEP,RST,OE,FR	6	V
VREF input voltage	VREF max	VREF	6	V
Allowable power dissipation	Pd max	*	3.35	W
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +150	°C

* Specified circuit board : 90mm× 90mm× 1.6mm, glass epoxy 2-layer board, with backside mounting.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage range	V_M	VM	9 to 55	V
Logic supply voltage range	VCC	VCC	2.7 to 5.5	V
Logic input voltage range	V_{IN}	ST,SCLK,SDATA,STB,STEP,RST,OE,FR	0 to VCC	V
VREF input voltage range	VREF	3.8V≤VCC≤5.5V	0 to 2.0	V
		2.7V≤VCC<3.8V	0 to VCC−1.8	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, VM = 48V, V_{CC} = 5V, VREF= 1.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Standby mode current	$I_M$stn	ST="L", with no load			1	μA
	ICCstn	ST="L", with no load			1	μA
Supply current	IM	ST="H",OE="L",RST="L", with no load		1.6	2.3	mA
	ICC	ST="H",OE="L",RST="L", with no load		1.7	2.3	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	210	°C
Thermal hysteresis width	ΔTSD	Design guarantee		40		°C
V_{CC} low voltage cutting voltage	Vthvc	Watching VCC pin voltage		2.3	2.45	V
VCC low voltage release voltage	Vrevc	Watching VCC pin voltage		2.5	2.7	V
V_M low voltage cutting voltage	Vthvm	Watching VM pin voltage		7.6	8.4	V
VM low voltage release voltage	Vrevm	Watching VM pin voltage		7.85	8.7	V
REG10 Output voltage	VREG1		9.4	10	10.6	V
VM-10V Output voltage	VREG2		37	38	39	V
Logic pin input current	I_{IN}L	ST,SCLK,SDATA,STB,STEP,RST,OE,FR V_{IN}=0.8V	4	8	12	μA
	I_{IN}H	ST,SCLK,SDATA,STB,STEP,RST,OE,FR V_{IN}=5V	30	50	70	μA

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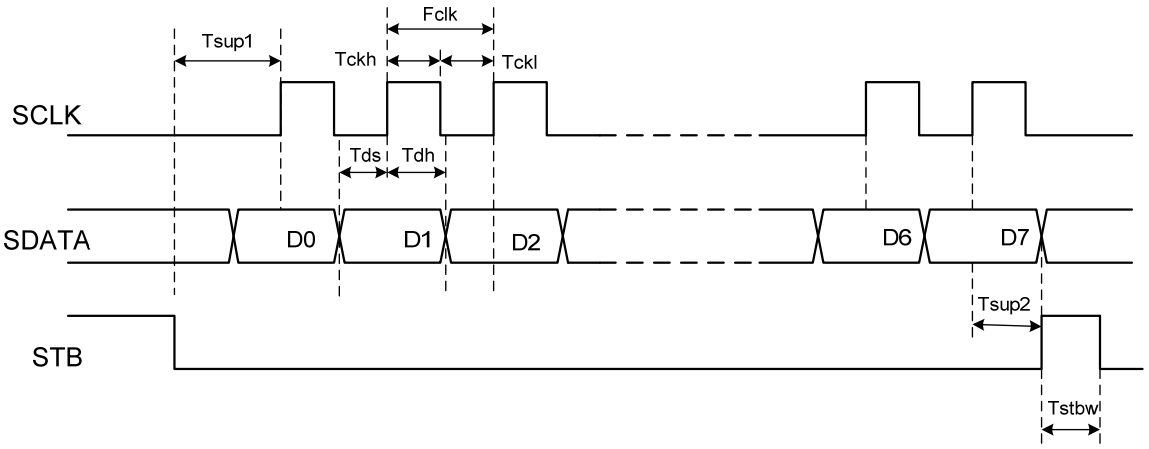
Parameter	Symbol	Conditions	min	typ	max	unit
Logic high-level input voltage	$V_{IN}H$	ST,SCLK,SDATA,STB,STEP,RST,OE,FR	2.0		5.5	V
Logic low-level input voltage	$V_{IN}H$		0		0.8	V
Chopping (PWM) period	Fchop1	D0=L,D1=H,D6=L,D7=L	6	8	10	μs
	Fchop2	D0=L,D1=H,D6=H,D7=L	12	16	20	μs
	Fchop3	D0=L,D1=H,D6=L,D7=H	18	24	30	μs
	Fchop4	D0=L,D1=H,D6=H,D7=H	24	32	40	μs
VREF pin input current	Iref	VREF=1.5V	−0.5		0	μA
Current setting comparator threshold voltage (current attenuation rate switching)	VRF000	D0=H,D1=L,D2=L,D3=L,D4=L	0.291	0.3	0.309	V
	VRF001	D0=H,D1=L,D2=H,D3=L,D4=L	0.261	0.27	0.279	V
	VRF010	D0=H,D1=L,D2=L,D3=H,D4=L	0.231	0.24	0.248	V
	VRF011	D0=H,D1=L,D2=H,D3=H,D4=L	0.201	0.21	0.218	V
	VRF100	D0=H,D1=L,D2=L,D3=L,D4=H	0.172	0.18	0.188	V
	VRF101	D0=H,D1=L,D2=H,D3=L,D4=H	0.142	0.15	0.158	V
	VRF110	D0=H,D1=L,D2=L,D3=H,D4=H	0.112	0.12	0.128	V
	VRF111	D0=H,D1=L,D2=H,D3=H,D4=H	0.082	0.09	0.098	V
SDO pin saturation voltage	Vsatsdo	Isdo=1mA			400	mV
MO pin saturation voltage	Vsatmo	Imo=1mA			400	mV
EMO pin saturation voltage	Vsatemo	Iemo=1mA			400	mV
STEP signal detection time	STEP1	D0=H,D1=L,D7=L	0.39	0.52	0.65	s
	STEP2	D0=H,D1=L,D7=H	0.78	1.04	1.3	s
High Side Output on resistance	RonH1	GU1,GU2,GU3,GU4-source Io=-10mA		20	32	Ω
	RonH2	GU1,GU2,GU3,GU4-sink Io=10mA		25	40	Ω
Low Side Output on resistance	RonL1	GB1,GB2,GB3,GB4-source side Io=-10mA		20	32	Ω
	RonL2	GB1,GB2,GB3,GB4-sink side Io=10mA		25	40	Ω
Serial Data Transfer Pin						
Minimum SCLK “H” pulse width	Tckh		0.125			μs
Minimum SCLK “L” pulse width	Tckl		0.125			μs
Minimum set up time (STB→SCLK rising edge)	Tsup1		0.125			μs
Minimum set up time (SCLK→STB rising edge)	Tsup2		0.125			μs
Minimum STB pulse width	Tstbw		0.125			μs
Data set up time	Tds		0.125			μs
Data hold time	Tdh		0.125			μs
Maximum SCLK frequency	Fclk				4	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

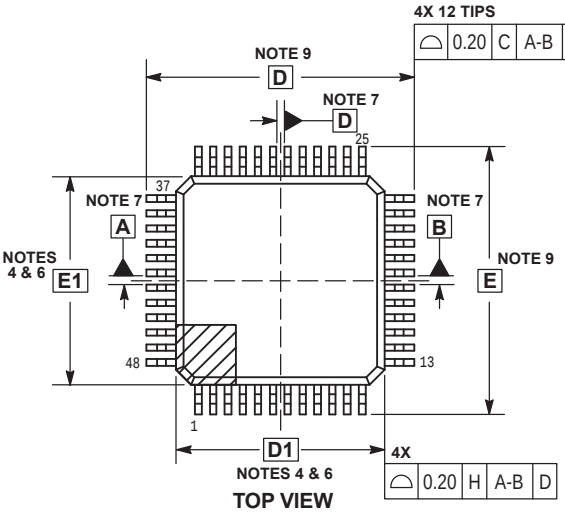
Serial input switching characteristics timing chart

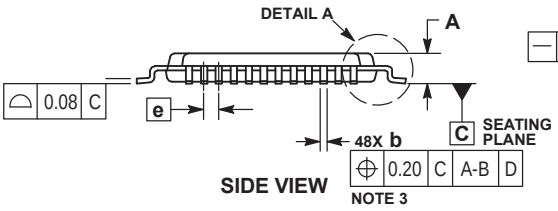


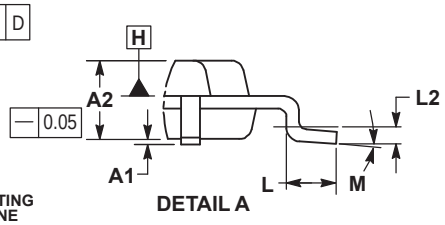
Package Dimensions

unit : mm

TQFP48 EP 7x7, 0.5P
CASE 932F
ISSUE C

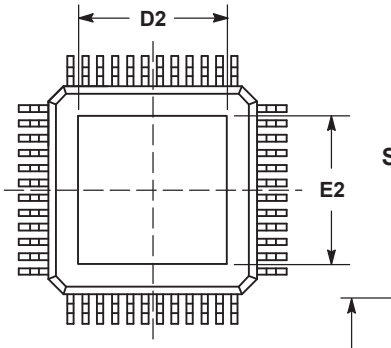




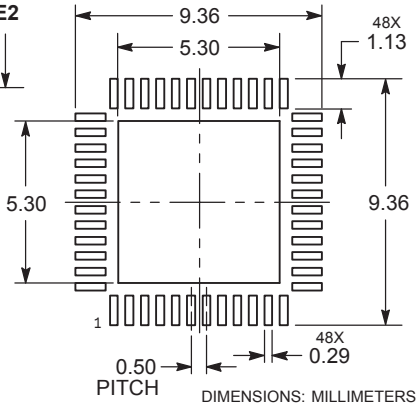


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN	MAX
A	0.95	1.25
A1	0.05	0.15
A2	0.90	1.20
b	0.17	0.27
D	9.00 BSC	
D1	7.00 BSC	
D2	4.90	5.10
E	9.00 BSC	
E1	7.00 BSC	
E2	4.90	5.10
e	0.50 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	7 °

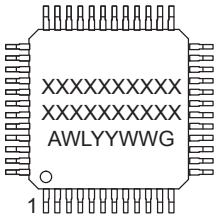


RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

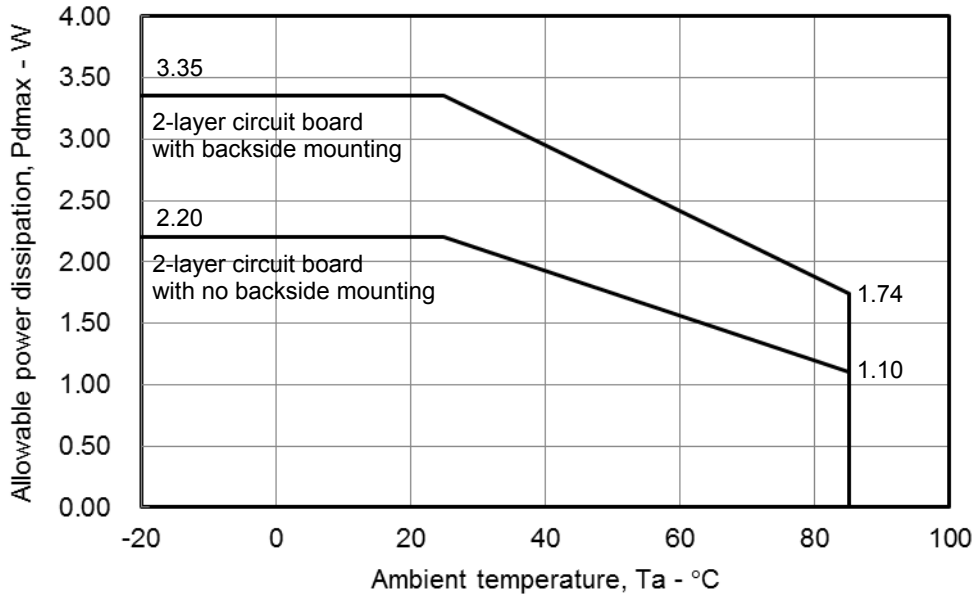


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

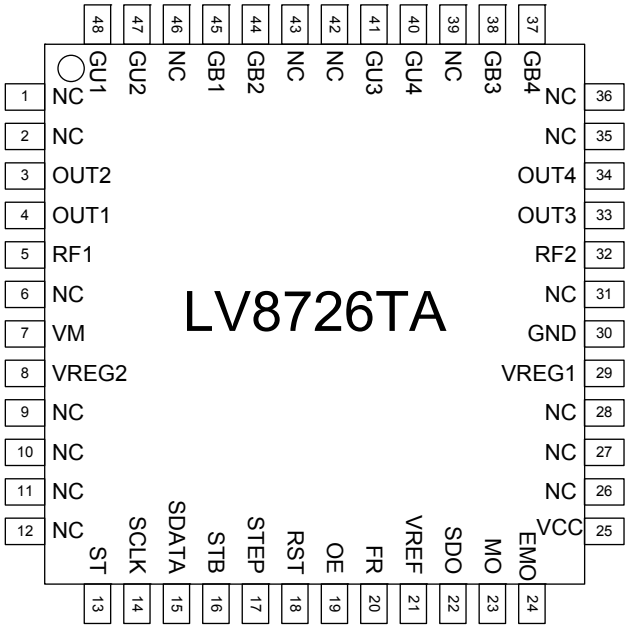
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

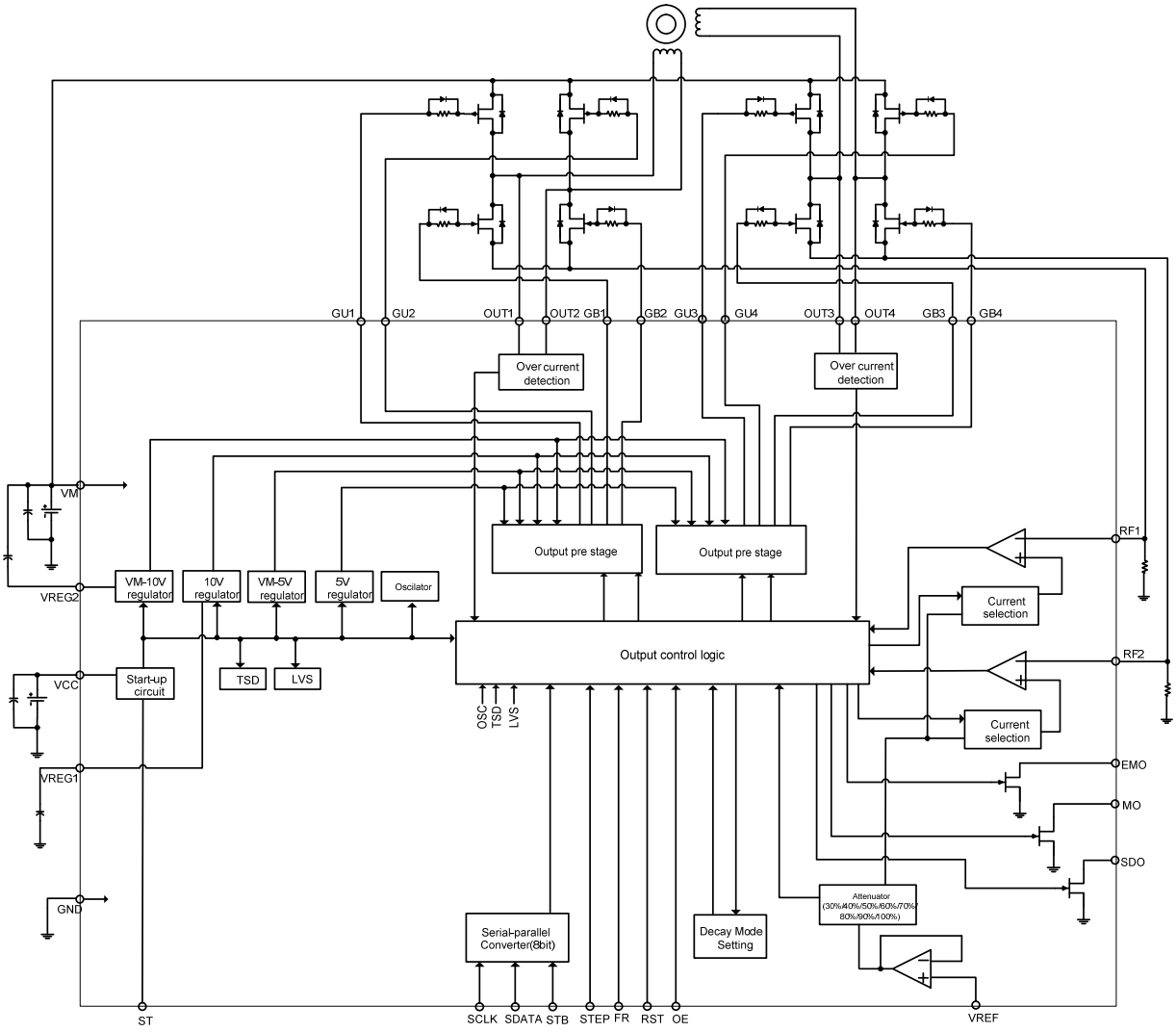
Pdmax - Ta



Pin Assignment



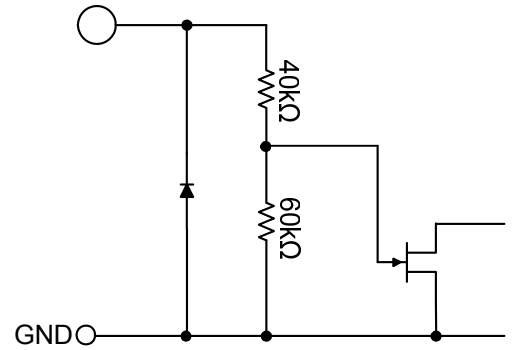
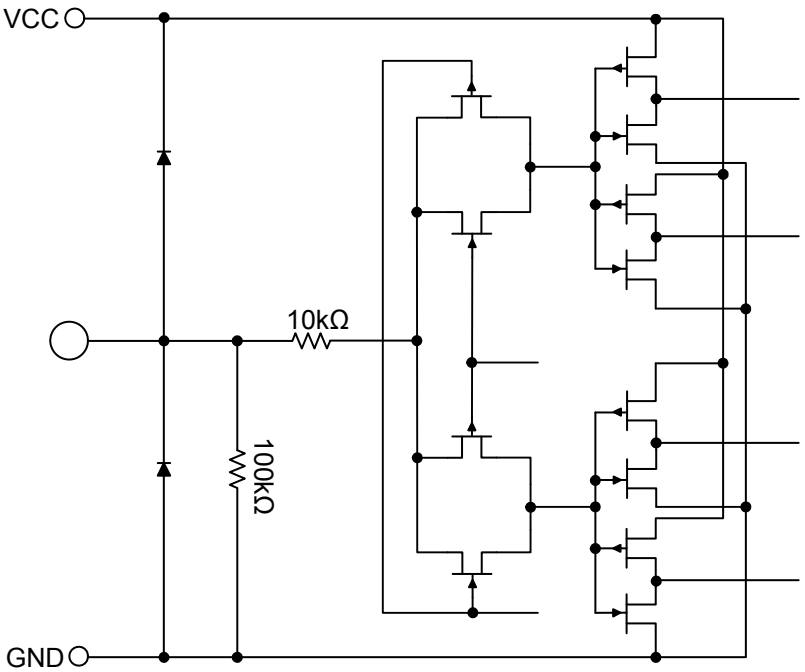
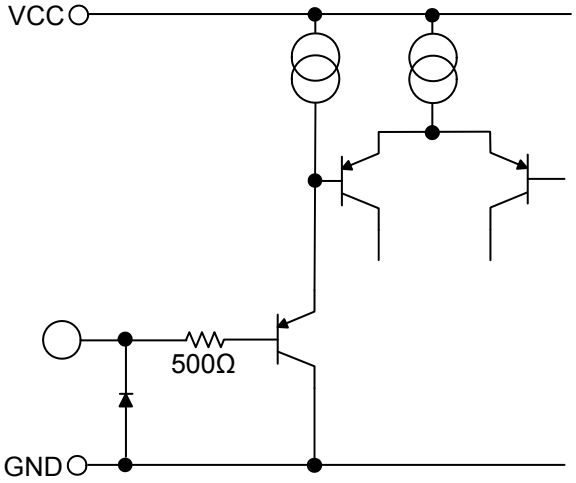
Block Diagram



Pin Functions

Pin No	Pin Name	Pin Function
3	OUT2	OUT2 voltage detection pin
4	OUT1	OUT1 voltage detection pin
5	RF1	Channel 1 Output current detection pin
7	VM	Motor power supply voltage pin
8	VREG2	Internal regulator capacitor connection pin for upper side FET drive
13	ST	Chip enable pin.
14	SCLK	Serial data transfer clock input
15	SDATA	Serial data input
16	STB	Serial data latch pulse input
17	STEP	Step clock pulse signal input pin
18	RST	Reset signal input pin
19	OE	Output enable signal input pin
20	FR	Forward / Reverse signal input pin
21	VREF	Constant-current control reference voltage input pin.
22	SDO	STEP detection output pin
23	MO	Position detecting monitor pin
24	EMO	Unusual condition warning output pins
25	VCC	Logic supply voltage pin
29	VREG1	Internal regulator capacitor connection pin for lower side FET drive
30	GND	GND pin
32	RF2	Channel 2 Output current detection pin
33	OUT3	OUT3 voltage detection pin
34	OUT4	OUT4 voltage detection pin
37	GB4	Output terminal for lower side gate drive 4
38	GB3	Output terminal for lower side gate drive 3
40	GU4	Output terminal for upper side gate drive 4
41	GU3	Output terminal for upper side gate drive 3
44	GB2	Output terminal for lower side gate drive 2
45	GB1	Output terminal for lower side gate drive 1
47	GU2	Output terminal for upper side gate drive 2
48	GU1	Output terminal for upper side gate drive 1
1,2,6,9, 10,11,12, 26,27,28, 31,35,36, 39,42,43, 46	NC	No connect

Equivalent Circuit

Pin No.	Pin Name	Equivalent Circuit
13	ST	
14 15 16 17 18 19 20	SCLK SDATA STB STEP RST OE FR	
21	VREF	

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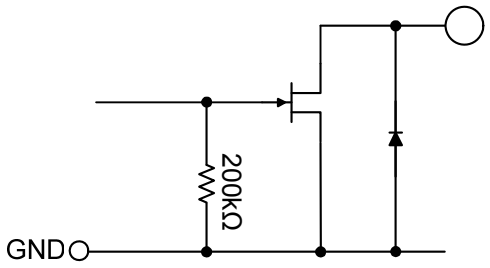
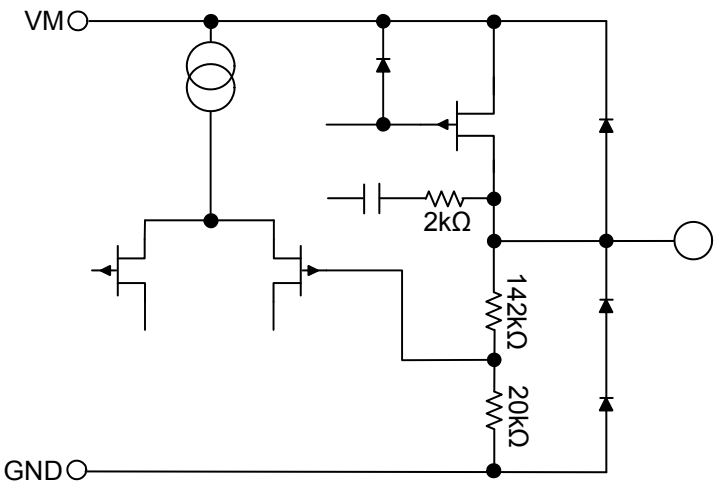
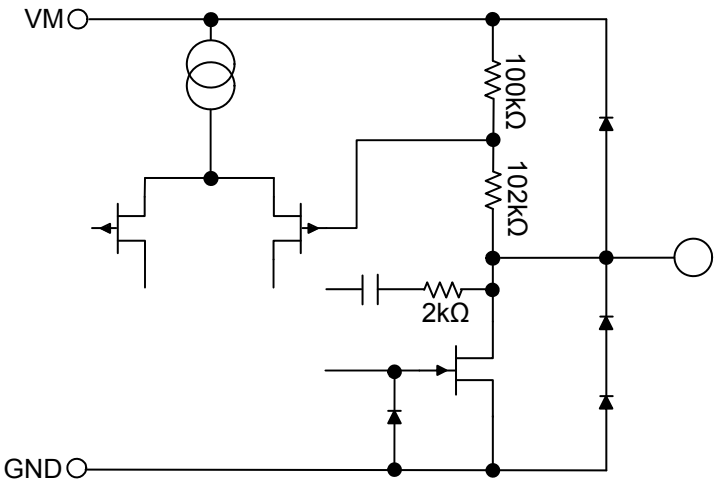
Pin No.	Pin Name	Equivalent Circuit
22 23 24	SDO MO EMO	
29	VREG1	
8	VREG2	

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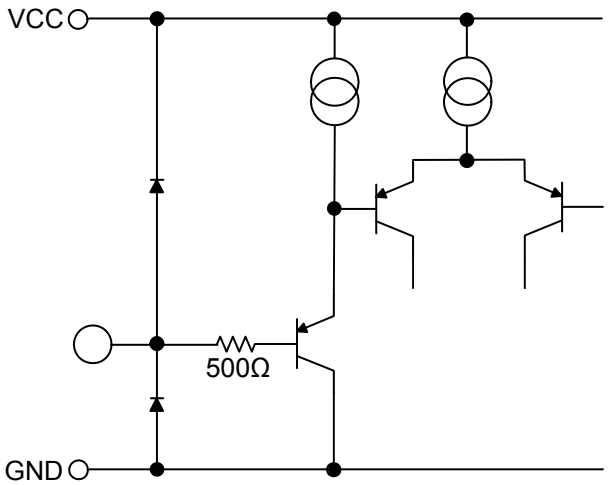
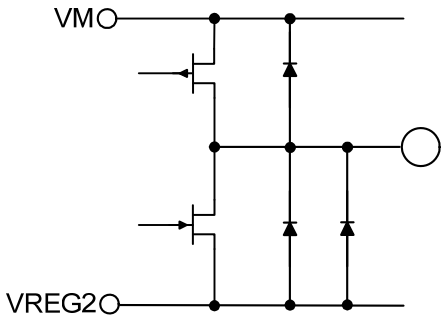
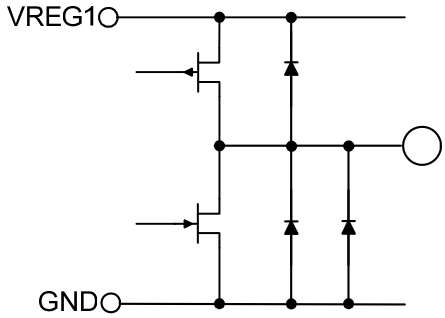
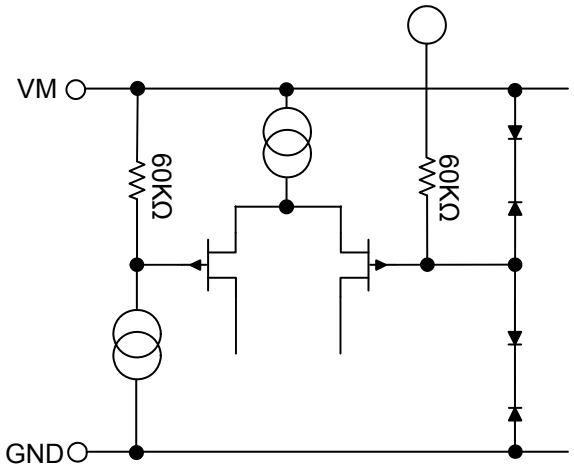
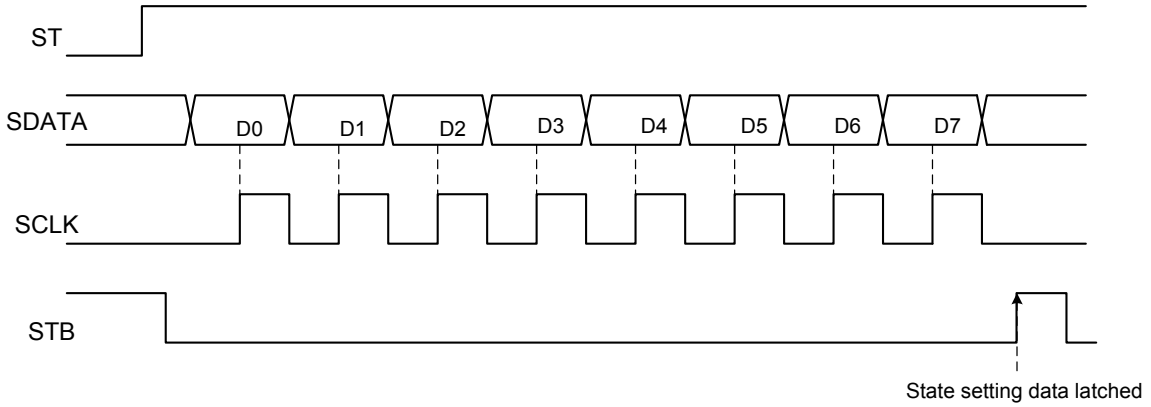
Pin No.	Pin Name	Equivalent Circuit
5 32	RF1 RF2	
40 41 47 48	GU4 GU3 GU2 GU1	
37 38 44 45	GB4 GB3 GB2 GB1	
3 4 33 34	OUT2 OUT1 OUT3 OUT4	

Description of operation

1. Serial Data Input Specifications

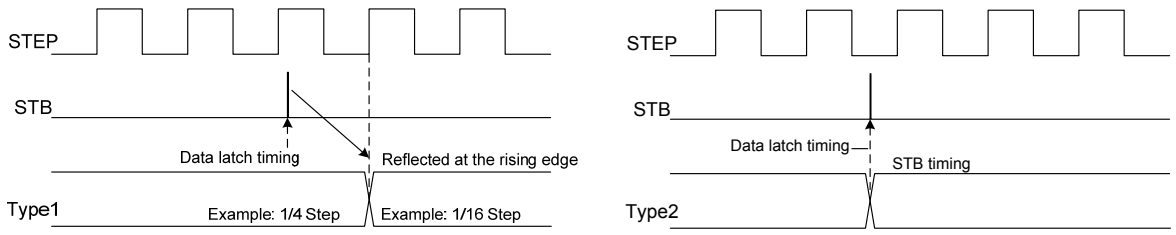
(1-1) Serial data input setup



The first of serial data communication, STB is set Low, and then input SDATA and SCLK signals. The SCLK signal is not accepted when STB is high.
SDATA inputs the data in the order of D0, D1, ... D6, D7.
Data is transferred on the rising edge of SCLK and after all data has been transferred, all data are latched on the rising edge of STB.

(1-2) Timing with which the Serial Data Settings are reflected at the Output

Type 1: After data latch, reflected by next STEP rising edge.
Step mode setting and Decay mode setting are reflected in a timing of type 1.
Type 2: Reflected at the same time as the STB signal data latch operation.
Current setting reference voltage attenuation ratio, chopping (PWM) period, blanking time, STEP signal detection time, over-current protection setting and EMO output setting are reflected in a timing of type 2.



Serial Data Truth Table 1

Input								Setting mode	Description	Serial data reflection timing	
D7	D6	D5	D4	D3	D2	D1	D0			STEP	STB
-	-	0	0	0	0	0	0	Step mode setting	1/2 Step	○	
-	-	0	0	0	1				1/4 Step		
-	-	0	0	1	0				1/8 Step		
-	-	0	0	1	1				1/16 Step		
-	-	0	1	0	0				1/32 Step		
-	-	0	1	0	1				1/64 Step		
-	-	0	1	1	0				1/128 Step		
-	-	0	1	1	1				1/3 Step		
-	-	1	0	0	0				1/6 Step		
-	-	1	0	0	1				1/12 Step		
-	-	1	0	1	0				1/36 Step		
-	-	1	0	1	1				1/5 Step		
-	-	1	1	0	0				1/10 Step		
-	-	1	1	0	1				1/20 Step		
-	-	1	1	1	0				1/50 Step		
-	-	1	1	1	1				1/100 Step		
0	0	-	-	-	-			EMO output setting	Over-current detection		○
-	-	-	-	-	-				-		
1	0	-	-	-	-				low voltage detection (VM pin voltage monitoring)		
1	1	-	-	-	-				TSD		
-	-	-	0	0	0	0	1	Current setting reference voltage attenuation ratio setting	100%		○
-	-	-	0	0	1				90%		
-	-	-	0	1	0				80%		
-	-	-	0	1	1				70%		
-	-	-	1	0	0				60%		
-	-	-	1	0	1				50%		
-	-	-	1	1	0				40%		
-	-	-	1	1	1				30%		
-	0	0	-	-	-			DECAY mode setting	MIXED DECAY (25% FAST)	○	
-	0	1	-	-	-				MIXED DECAY (50% FAST)		
-	1	0	-	-	-				SLOW DECAY		
-	1	1	-	-	-				FAST DECAY		
0	-	-	-	-	-			STEP signal detection time setting	0.52s		○
1	-	-	-	-	-				1.04s		

Serial Data Truth Table 2

Input								Setting mode	Description	Serial data reflection timing	
D7	D6	D5	D4	D3	D2	D1	D0			STEP	STB
-	-	-	-	0	0	1	0	Blanking time setting	0.5μs		○
-	-	-	-	0	1				1.0μs		
-	-	-		1	0				2.0μs		
-	-	-		1	1				4.0μs		
-	-	0	0		-			Through current protector OFF time setting	0.5μs		○
-	-	0	1		-				1.0μs		
-		1	0	-	-				2.0μs		
-		1	1	-	-				4.0μs		
0	0		-	-	-			chopping (PWM) period setting	8μs		○
0	1		-	-	-				16μs		
1	0	-	-	-	-				24μs		
1	1	-	-	-	-				32μs		
-	-	-	-	-	0	1	1	Over-current protection setting	ON		○
-	-	-	-	-	1				OFF (Disable over-current protection)		
-	-	-	-	0	-				Latch type		
-	-	-	-	1	-				Auto reset type		
-	-	-	-	-	-			-	-	-	-
-	-	-	-	-	-				-		
-	-	-	-	-	-				-		
-	-	-	-	-	-				-		
-	-	-	-	-	-			-	-	-	-
-	-	-	-	-	-				-		
-	-	-	-	-	-				-		
-	-	-	-	-	-				-		

2. Reference describing operation

(2-1) Standby function (ST)

When ST pin is Low, the IC enters standby mode, all logic is reset and output is turned OFF.
When ST pin is High, the standby mode is released.

(2-2) STEP pin function (STEP)

STEP input advances electrical angle at every rising edge (advances step by step) .

Input		Operating mode
ST	STEP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

(2-3) Excitation setting method (D0="0", D1="0")

Set the micro step resolution as shown below table by serial data setting.

Input				Micro step resolution (STEP)	Initial position	
D5	D4	D3	D2		1ch current	2ch current
0	0	0	0	1/2	100%	0%
0	0	0	1	1/4	100%	0%
0	0	1	0	1/8	100%	0%
0	0	1	1	1/16	100%	0%
0	1	0	0	1/32	100%	0%
0	1	0	1	1/64	100%	0%
0	1	1	0	1/128	100%	0%
0	1	1	1	1/3	100%	0%
1	0	0	0	1/6	100%	0%
1	0	0	1	1/12	100%	0%
1	0	1	0	1/36	100%	0%
1	0	1	1	1/5	100%	0%
1	1	0	0	1/10	100%	0%
1	1	0	1	1/20	100%	0%
1	1	1	0	1/50	100%	0%
1	1	1	1	1/100	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each micro step resolution.

(2-4) Position detection monitoring function (MO)

The MO position detection monitoring pin is an open drain type.
When the excitation position is in the initial position, the MO output is placed in the ON state.
(Refer to "Examples of current waveforms in each of the excitation modes.")

(2-5) Constant-current setting

The constant-current control setting consist of the VREF voltage setting and RF1(2) resistor connected between RF1(2) and ground. The current is set according to the following equation.

IOUT [A] = (VREF [V] / 5) / RF1 (2) [Ω]

Also, the voltage applied to the VREF pin can be switched to eight stages settings by the serial data setting. This function is effective for power saving when the motor holding current is applied.

Attenuation function of the VREF input voltage. (D0="1", D1="0")

D4	D3	D2	Current setting reference voltage attenuation ratio
0	0	0	100%
0	0	1	90%
0	1	0	80%
0	1	1	70%
1	0	0	60%
1	0	1	50%
1	1	0	40%
1	1	1	30%

The output current calculation method for using of attenuation function of the VREF input voltage is as below.

I_{OUT} = (VREF / 5) × Attenuation ratio / RF resistance

e.g. When the VREF is 1.5V and the set reference voltage is 100% and the RF resistance is 0.1Ω, the following output current is set.

I_{OUT} = 1.5 / 5 × 100% / 0.1Ω = 3.0A

In this conditions, when 50% is set to reference voltage attenuation ratio,

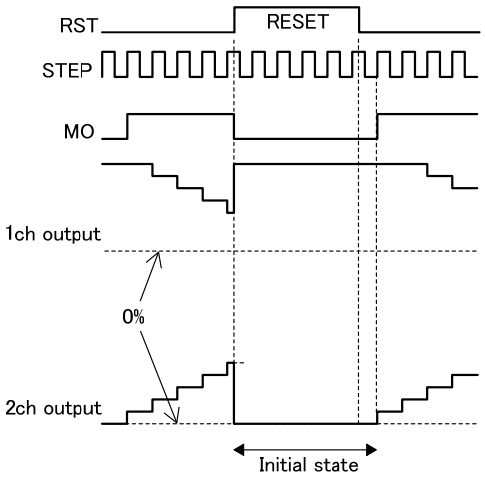
I_{OUT} = 1.5 / 5 × 50% / 0.1Ω = 1.5A

Therefore, the power saving is executable by attenuation of the output current when motor holding current is supplied.

(2-6) Reset function (RST)

When the RST pin is set High, the output goes to initial mode and excitation position is fixed in the initial position for STEP pin and FR pin input. MO pin outputs at low levels at the initial position. (Open drain connection)

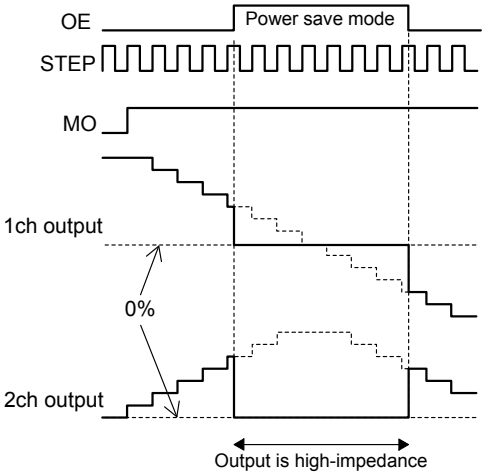
RST	Operating mode
Low	Normal operation
High	Reset state



(2-7) Output enable function (OE)

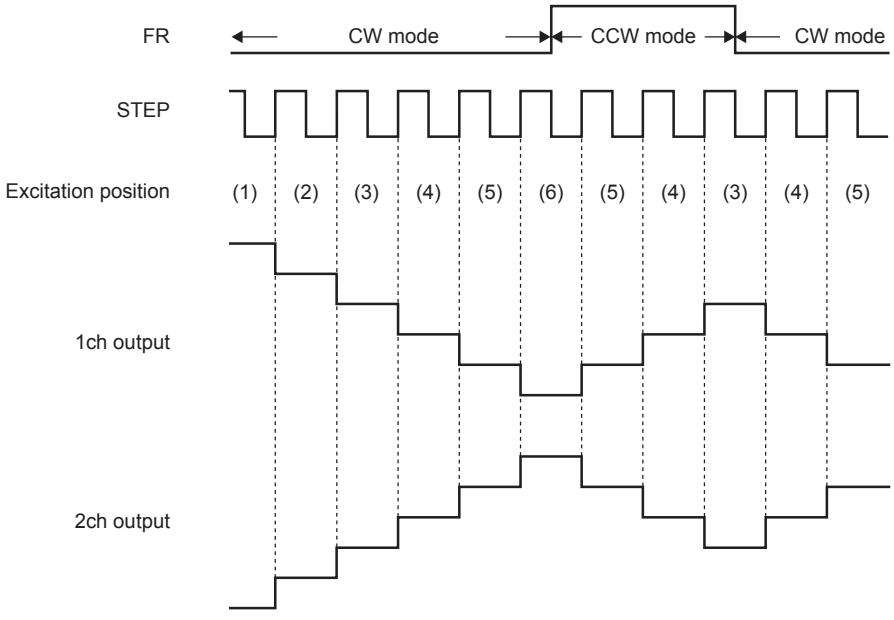
When the OE pin is set High, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STEP is input. Therefore, when OE pin is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

OE	Operating mode
Low	Output ON
High	Output OFF



(2-8) Forward / reverse switching function (FR)

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the STEP pin. In addition, CW and CCW mode are switched by FR pin setting.

In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.

In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(2-9) DECAY mode setting

Current DECAY method is selectable as shown below by the serial data setting.

DECAY mode setting (D0="1", D1="0")

D6	D5	DECAY mode
0	0	MIXED DECAY (25%FAST)
0	1	MIXED DECAY (50%FAST)
1	0	SLOW DECAY
1	1	FAST DECAY

(2-10) Blanking time setting

If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the RF pin, and this may result in erroneous detection. To prevent this erroneous detection, a blanking period is provided to prevent the noise occurring during mode switching from being received. During this period, the mode is not switched from charge to decay even if noise is carried on the RF pin.

Blanking time is selectable as shown below by the serial data setting.

Blanking time setting (D0="0", D1="1")

D3	D2	Blanking time setting
0	0	0.5μs
0	1	1.0μs
1	0	2.0μs
1	1	4.0μs

(2-11) Through current protector OFF time setting

This IC establishes the OFF time so as not to turn ON upper and lower side FET at the same time.

Through current protector OFF time is selectable as shown below by the serial data setting.

Through current protector OFF time setting (D0="0", D1="1")

D5	D4	Through current protector OFF time
0	0	0.5μs
0	1	1.0μs
1	0	2.0μs
1	1	4.0μs

(2-12) Chopping (PWM) period setting

For constant-current control, this IC performs chopping operations at the frequency determined by the serial data setting.

Chopping (PWM) period setting (D0="0", D1="1")

D7	D6	Chopping (PWM) period
0	0	8μs
0	1	16μs
1	0	24μs
1	1	32μs

(2-13) STEP detection output (SDO)

The SDO pin is an open-drain output.

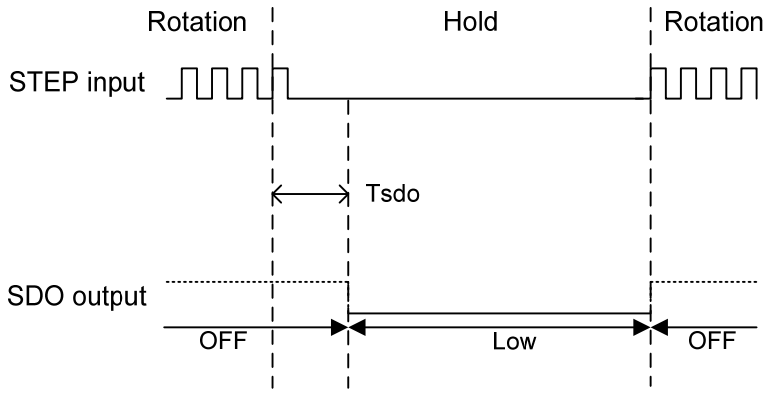
When STEP signal is not input more than detection time, the open-drain is turned ON and output level is Low.

The open-drain was turned ON one time, it is turned OFF by inputting STEP signal again.

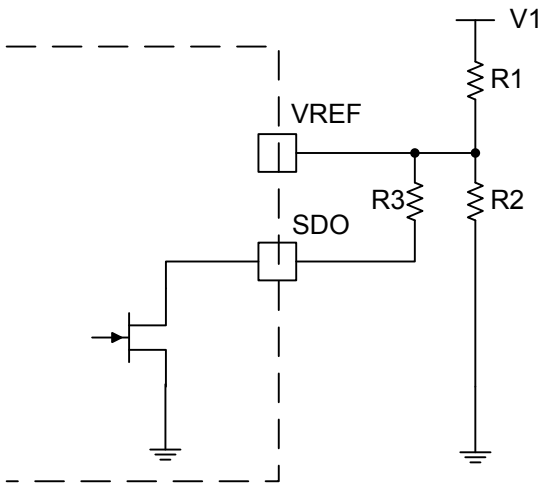
STEP signal detection time (Tsdo) is set as shown below by serial data setting.

STEP signal detection time setting (D0="1", D1="0")

D7	STEP signal detection time
0	0.52s
1	1.04s



By connecting circumference parts like the example of the following circuit diagram using a SDO pin, that is a STEP signal is not inputted more than detection time, it is a SDO output's turning on in the state of holding turning on electricity the position of a stepping motor, and setting current's falling because VREF input voltage's falls, and stopping power consumption — it can do.



(Example) When V1=5V, R1=27kΩ, R2=4.7kΩ, R3=1kΩ, the VREF input voltage is shown below.

SDO output OFF: VREF = V1 × R2 / (R1+R2) = 0.741V

SDO output ON: VREF = V1 × (R2//R3) / (R1+ (R2//R3)) = 0.126V

(2-14) Over-current protection

The LV8726TA incorporates an over-current protection circuit that, when the output has been shorted by an event such as shorting to power or shorting to ground, sets the output to OFF mode in order to prevent the IC from being damaged. As for the detection level of upper side Pch MOSFET, the voltage between drain and source is approximately 3V. As for the detection level of lower side Nch MOSFET, the voltage is set the following equation by constant current(Iout) and RF1(2) resistor connected between RF1(2) and ground.

Detection level of lower side Nch MOSFET: Vocpl

Vocpl [V] ≈ Iout [A] × RF1(2) resistor [Ω] × 3

e.g. When the Iout is 3.0A and the set reference voltage is 100% and RF resistance is 0.1Ω

Vocpl ≈ 3.0A × 0.1Ω × 3 = 0.9V

Over-current protection is set as shown below by serial data setting

Over-current protection setting (D0="1", D1="1")

D2	State
0	Over-current protection ON
1	Over-current protection OFF

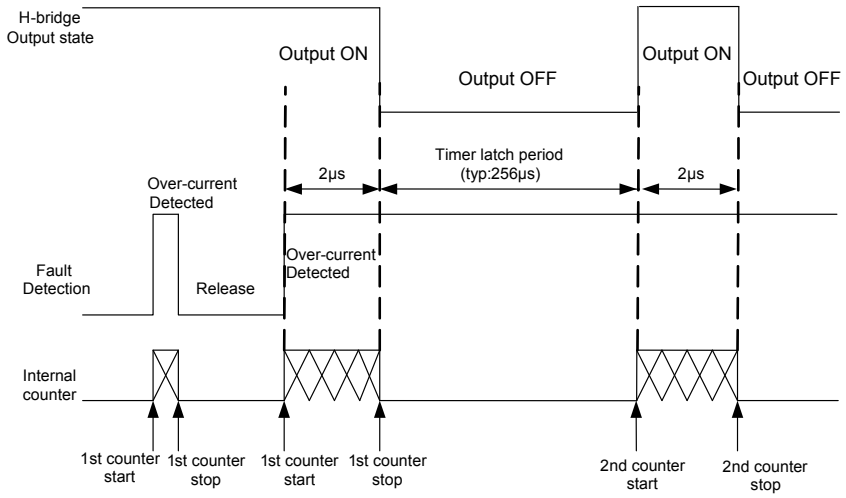
When a state of over-current protection is ON, the detection mode of it can change like the following table by serial data setting.

Over-current protection mode setting (D0="1", D1="1")

D3	Mode
0	Latch type
1	Auto reset type

(2-14-1) Latch type

In the latch mode, when the output current exceeds the detection current level, the output is turned OFF. When over-current is detected for 2μs, over-current detection circuit is operating and output is once turned OFF. Subsequently, the output is turned ON again after the timer latch period (typ. 256μs). If the output remains in over-current condition, it is turned OFF again, and fix the output state to OFF mode, and EMO output is turned ON.
When output is fixed in OFF mode by over-current protection, this state is released by setting ST = "L".



(2-14-2) Auto reset type

In the automatic reset mode, when the over-current protection is operating, the output waveform changes to the switching waveform.

As with the latch system, when the over-current condition is detected, the over-current protection circuit is activated. When the operation of the over-current detection circuit exceeds the timer latch time (2μs) described later, the output is changed over to the OFF mode and is reset to the ON mode again in 2ms (typ). In this event, if the over-current mode still continues, the switching mode described above is repeated until the over-current mode is canceled.

(2-15) Unusual condition warning output pins (EMO)

The LV8726TA is provided with the EMO pin which notifies the CPU of an unusual condition if the protection circuit operates by detecting an unusual condition of the IC. This pin is of the open-drain output type and when an unusual condition is detected, the EMO output is placed in the ON (EMO = Low) state.

EMO output is selectable as shown below by the serial data setting.

EMO output setting (D0="0", D1="0")

D7	D6	EMO output	Notes
0	0	Over-current detection	(1)
-	-	-	
1	0	Low voltage detection (VM pin voltage monitoring)	(2)
1	1	TSD	

*Notes

(1) Shorting-to-power, shorting-to-ground, or shorting-to-load occurs at the output pin and the over-current protection circuit is activated.

(2) When the VM voltage was less than 8V, a low voltage protection circuit is activated.

(2-16) Thermal shutdown circuit function

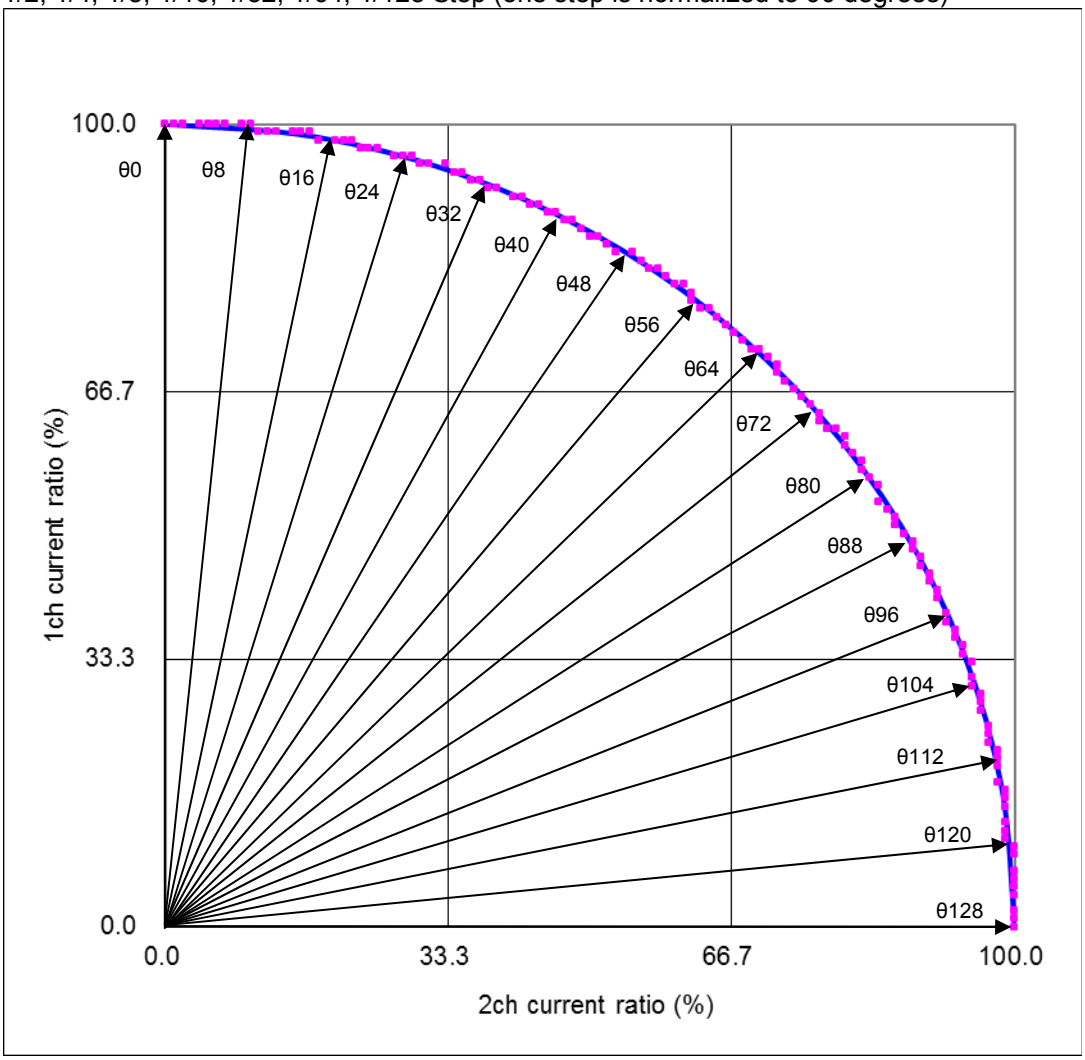
The Thermal shutdown circuit is built into, and the output is turned off when junction temperature Tj exceeds 180˚C. The value of hysteresis and when it falls, the temperature drives the output again (automatic restoration).

The overheating protection circuit doesn't secure protection and the destruction prevention of the set because it becomes operation by the area where ratings Tjmax=150˚C of the junction temperature was exceeded.

TSD = 180˚C (typ)

ΔTSD = 40˚C (typ)

(2-17) Output current vector locus
1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 Step (one step is normalized to 90 degrees)

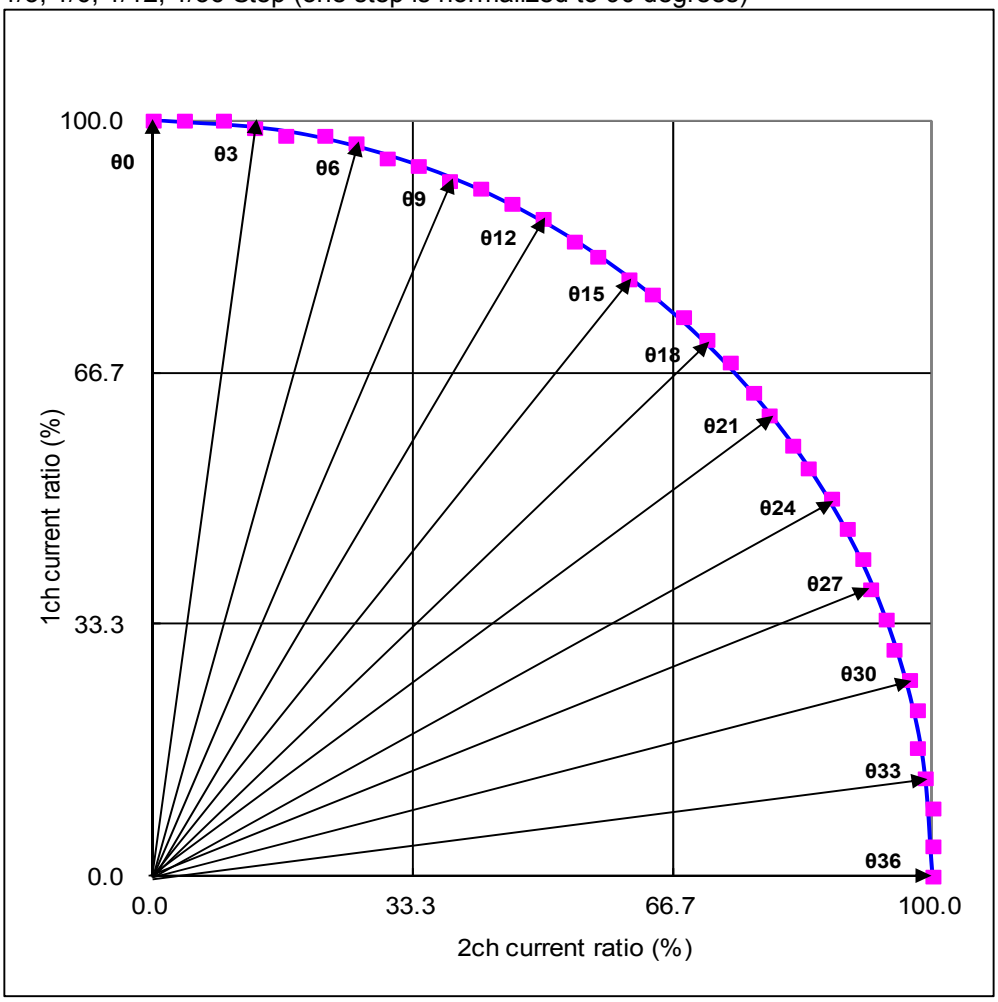


Current setting ratio in each micro step resolution

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 Step

	1/128 Step		1/64 Step		1/32 Step		1/16 Step		1/8 Step		1/4 Step		1/2 Step			1/128 Step		1/64 Step		1/32 Step		1/16 Step		1/8 Step		1/4 Step		1/2 Step	
STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0	θ65	70	72												
θ1	100	1													θ66	69	72	69	72										
θ2	100	2	100	2											θ67	68	73												
θ3	100	4													θ68	67	74	67	74	67	74								
θ4	100	5	100	5	100	5									θ69	66	75												
θ5	100	6													θ70	65	76	65	76										
θ6	100	7	100	7											θ71	64	77												
θ7	100	9													θ72	63	77	63	77	63	77	63	77						
θ8	100	10	100	10	100	10	100	10							θ73	62	78												
θ9	99	11													θ74	62	79	62	79										
θ10	99	12	99	12											θ75	61	80												
θ11	99	13													θ76	60	80	60	80	60	80								
θ12	99	15	99	15	99	15									θ77	59	81												
θ13	99	16													θ78	58	82	58	82										
θ14	99	17	99	17											θ79	57	82												
θ15	98	18													θ80	56	83	56	83	56	83	56	83	56	83				
θ16	98	20	98	20	98	20	98	20	98	20					θ81	55	84												
θ17	98	21													θ82	53	84	53	84										
θ18	98	22	98	22											θ83	52	85												
θ19	97	23													θ84	51	86	51	86	51	86								
θ20	97	24	97	24	97	24									θ85	50	86												
θ21	97	25													θ86	49	87	49	87										
θ22	96	27	96	27											θ87	48	88												
θ23	96	28													θ88	47	88	47	88	47	88	47	88						
θ24	96	29	96	29	96	29	96	29							θ89	46	89												
θ25	95	30													θ90	45	89	45	89										
θ26	95	31	95	31											θ91	44	90												
θ27	95	33													θ92	43	90	43	90	43	90								
θ28	94	34	94	34	94	34									θ93	42	91												
θ29	94	35													θ94	41	91	41	91										
θ30	93	36	93	36											θ95	39	92												
θ31	93	37													θ96	38	92	38	92	38	92	38	92	38	92	38	92		
θ32	92	38	92	38	92	38	92	38	92	38	92	38			θ97	37	93												
θ33	92	39													θ98	36	93	36	93										
θ34	91	41	91	41											θ99	35	94												
θ35	91	42													θ100	34	94	34	94	34	94								
θ36	90	43	90	43	90	43									θ101	33	95												
θ37	90	44													θ102	31	95	31	95										
θ38	89	45	89	45											θ103	30	95												
θ39	89	46													θ104	29	96	29	96	29	96	29	96						
θ40	88	47	88	47	88	47	88	47							θ105	28	96												
θ41	88	48													θ106	27	96	27	96										
θ42	87	49	87	49											θ107	25	97												
θ43	86	50													θ108	24	97	24	97	24	97								
θ44	86	51	86	51	86	51									θ109	23	97												
θ45	85	52													θ110	22	98	22	98										
θ46	84	53	84	53											θ111	21	98												
θ47	84	55													θ112	20	98	20	98	20	98	20	98	20	98				
θ48	83	56	83	56	83	56	83	56	83	56					θ113	18	98												
θ49	82	57													θ114	17	99	17	99										
θ50	82	58	82	58											θ115	16	99												
θ51	81	59													θ116	15	99	15	99	15	99								
θ52	80	60	80	60	80	60									θ117	13	99												
θ53	80	61													θ118	12	99	12	99										
θ54	79	62	79	62											θ119	11	99												
θ55	78	62													θ120	10	100	10	100	10	100	10	100						
θ56	77	63	77	63	77	63	77	63							θ121	9	100												
θ57	77	64													θ122	7	100	7	100										
θ58	76	65	76	65											θ123	6	100												
θ59	75	66													θ124	5	100	5	100	5	100								
θ60	74	67	74	67	74	67									θ125	4	100												
θ61	73	68													θ126	2	100	2	100										
θ62	72	69	72	69											θ127	1	100												
θ63	72	70													θ128	0	100	0	100	0	100	0	100	0	100	0	100	0	100
θ64	71	71	71	71	71	71	71	71	71	71	71	71	71	71															

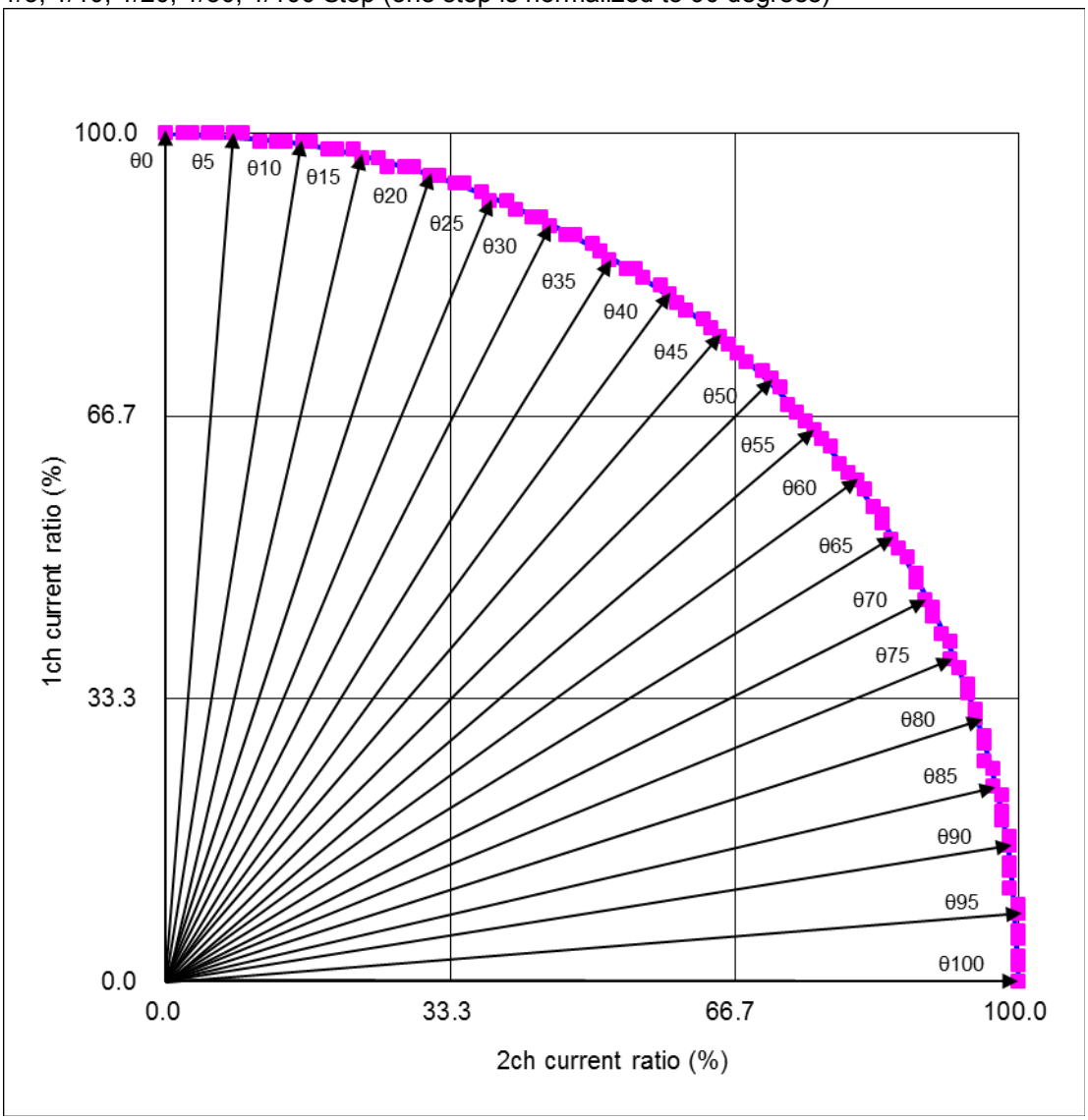
Output current vector locus
1/3, 1/6, 1/12, 1/36 Step (one step is normalized to 90 degrees)



Current setting ratio in each micro step resolution
1/3, 1/6, 1/12, 1/36 Step

	1/36 Step		1/12 Step		1/6 Step		1/3 Step			1/36 Step		1/12 Step		1/6 Step		1/3 Step	
STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	θ19	68	74						
θ1	100	4							θ20	64	77						
θ2	100	9							θ21	61	79	61	79				
θ3	99	13	99	13					θ22	57	82						
θ4	98	17							θ23	54	84						
θ5	98	22							θ24	50	87	50	87	50	87	50	87
θ6	97	26	97	26	97	26			θ25	46	89						
θ7	95	30							θ26	42	91						
θ8	94	34							θ27	38	92	38	92				
θ9	92	38	92	38					θ28	34	94						
θ10	91	42							θ29	30	95						
θ11	89	46							θ30	26	97	26	97	26	97		
θ12	87	50	87	50	87	50	87	50	θ31	22	98						
θ13	84	54							θ32	17	98						
θ14	82	57							θ33	13	99	13	99				
θ15	79	61	79	61					θ34	9	100						
θ16	77	64							θ35	4	100						
θ17	74	68							θ36	0	100	0	100	0	100	0	100
θ18	71	71	71	71	71	71											

Output current vector locus
1/5, 1/10, 1/20, 1/50, 1/100 Step (one step is normalized to 90 degrees)

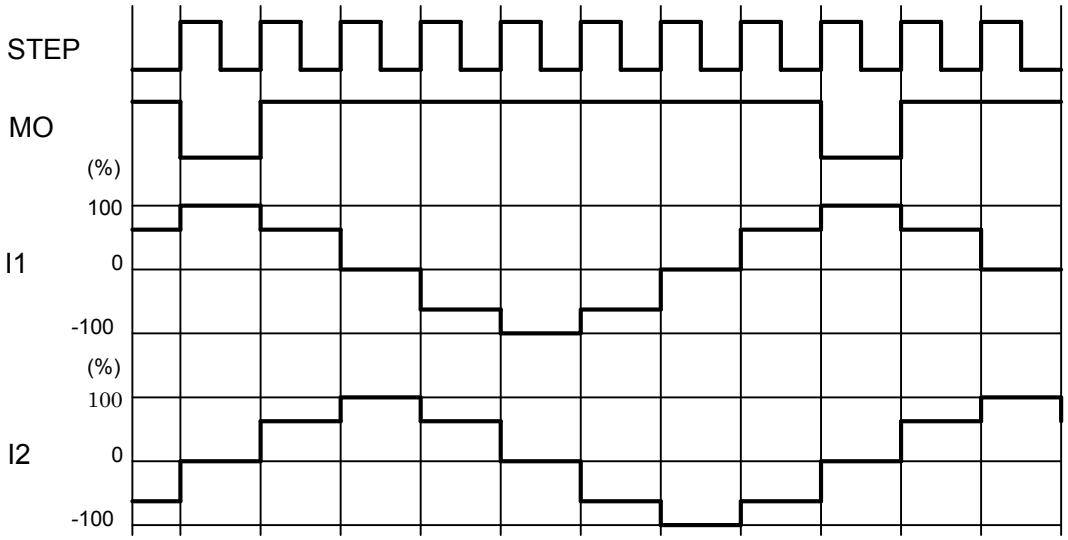


Current setting ratio in each micro step resolution
1/5, 1/10, 1/20, 1/50, 1/100 Step

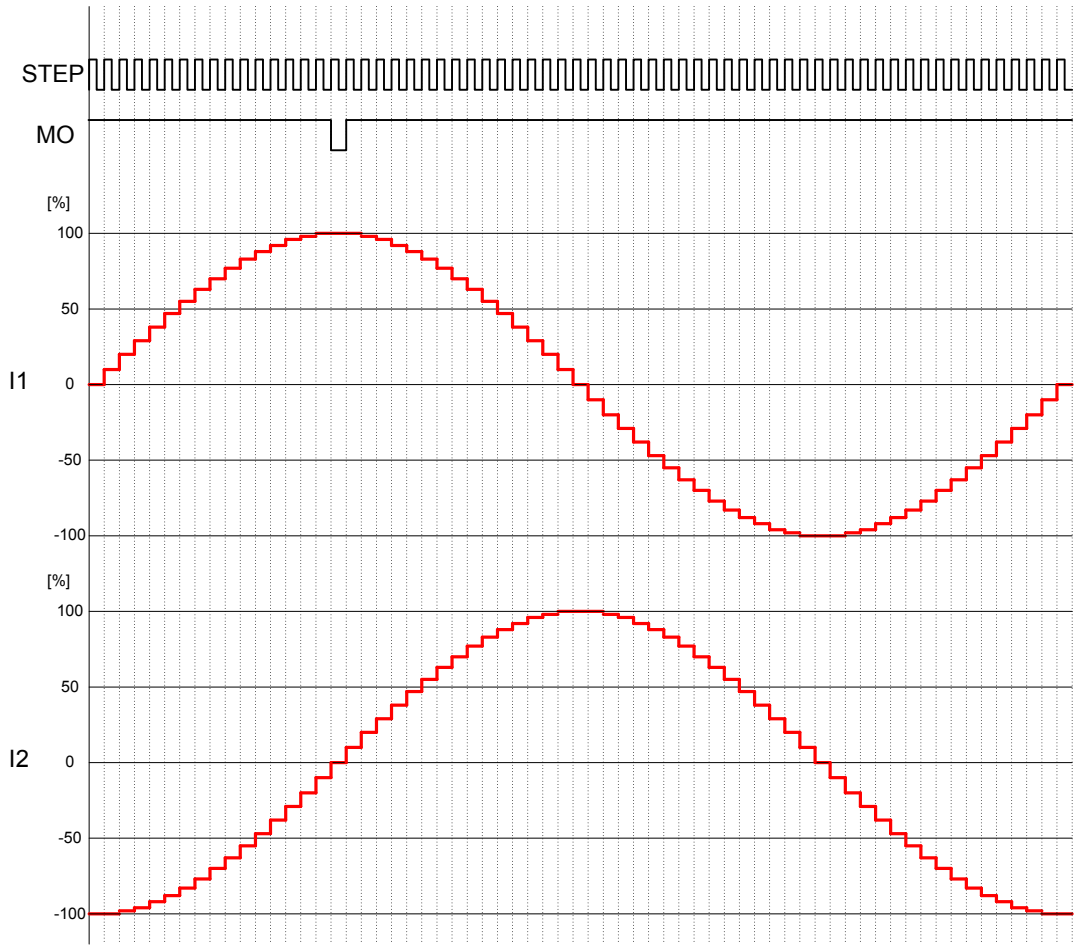
	1/100 Step		1/50 Step		1/20 Step		1/10 Step		1/5 Step			1/100 Step		1/50 Step		1/20 Step		1/10 Step		1/5 Step	
STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	STEP	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	100	0	θ51	70	72								
θ1	100	2									θ52	68	73	68	73						
θ2	100	3	100	3							θ53	67	74								
θ3	100	5									θ54	66	75	66	75						
θ4	100	6	100	6							θ55	65	76			65	76				
θ5	100	8			100	8					θ56	64	77	64	77						
θ6	100	9	100	9							θ57	63	78								
θ7	99	11									θ58	61	79	61	79						
θ8	99	13	99	13							θ59	60	80								
θ9	99	14									θ60	59	81	59	81	59	81	59	81	59	81
θ10	99	16	99	16	99	16	99	16			θ61	58	82								
θ11	99	17									θ62	56	83	56	83						
θ12	98	19	98	19							θ63	55	84								
θ13	98	20									θ64	54	84	54	84						
θ14	98	22	98	22							θ65	52	85			52	85				
θ15	97	23			97	23					θ66	51	86	51	86						
θ16	97	25	97	25							θ67	50	87								
θ17	96	26									θ68	48	88	48	88						
θ18	96	28	96	28							θ69	47	88								
θ19	96	29									θ70	45	89	45	89	45	89	45	89		
θ20	95	31	95	31	95	31	95	31	95	31	θ71	44	90								
θ21	95	32									θ72	43	90	43	90						
θ22	94	34	94	34							θ73	41	91								
θ23	94	35									θ74	40	92	40	92						
θ24	93	37	93	37							θ75	38	92			38	92				
θ25	92	38			92	38					θ76	37	93	37	93						
θ26	92	40	92	40							θ77	35	94								
θ27	91	41									θ78	34	94	34	94						
θ28	90	43	90	43							θ79	32	95								
θ29	90	44									θ80	31	95	31	95	31	95	31	95	31	95
θ30	89	45	89	45	89	45	89	45			θ81	29	96								
θ31	88	47									θ82	28	96	28	96						
θ32	88	48	88	48							θ83	26	96								
θ33	87	50									θ84	25	97	25	97						
θ34	86	51	86	51							θ85	23	97			23	97				
θ35	85	52			85	52					θ86	22	98	22	98						
θ36	84	54	84	54							θ87	20	98								
θ37	84	55									θ88	19	98	19	98						
θ38	83	56	83	56							θ89	17	99								
θ39	82	58									θ90	16	99	16	99	16	99	16	99		
θ40	81	59	81	59	81	59	81	59	81	59	θ91	14	99								
θ41	80	60									θ92	13	99	13	99						
θ42	79	61	79	61							θ93	11	99								
θ43	78	63									θ94	9	100	9	100						
θ44	77	64	77	64							θ95	8	100			8	100				
θ45	76	65			76	65					θ96	6	100	6	100						
θ46	75	66	75	66							θ97	5	100								
θ47	74	67									θ98	3	100	3	100						
θ48	73	68	73	68							θ99	2	100								
θ49	72	70									θ100	0	100	0	100	0	100	0	100	0	100
θ50	71	71	71	71	71	71	71	71													

(2-18) Current wave example in each micro step resolution.
(1/2 STEP, 1/16 STEP, 1/128 SETP, 1/12 STEP, 1/50 STEP)

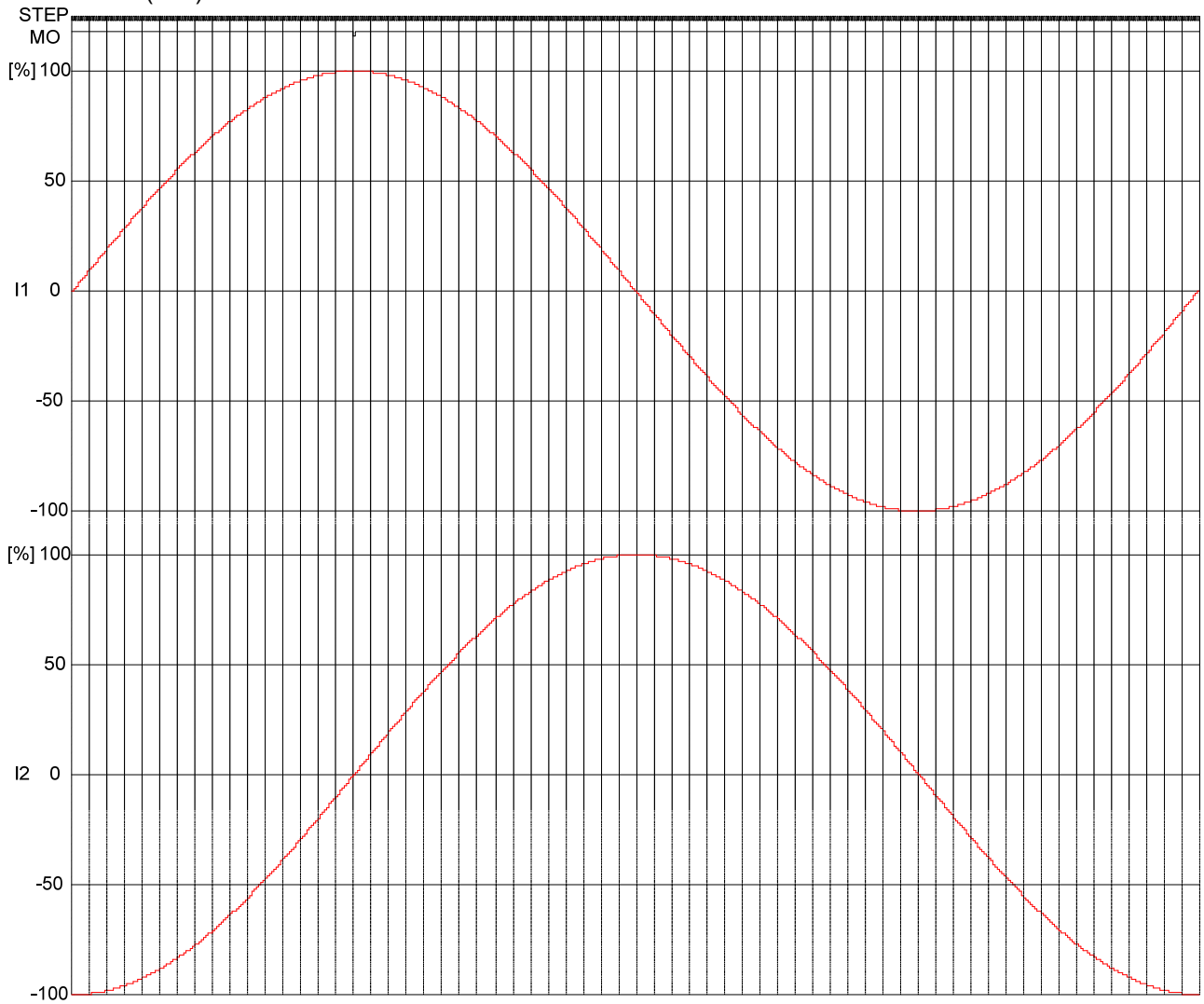
1/2 STEP (CW)



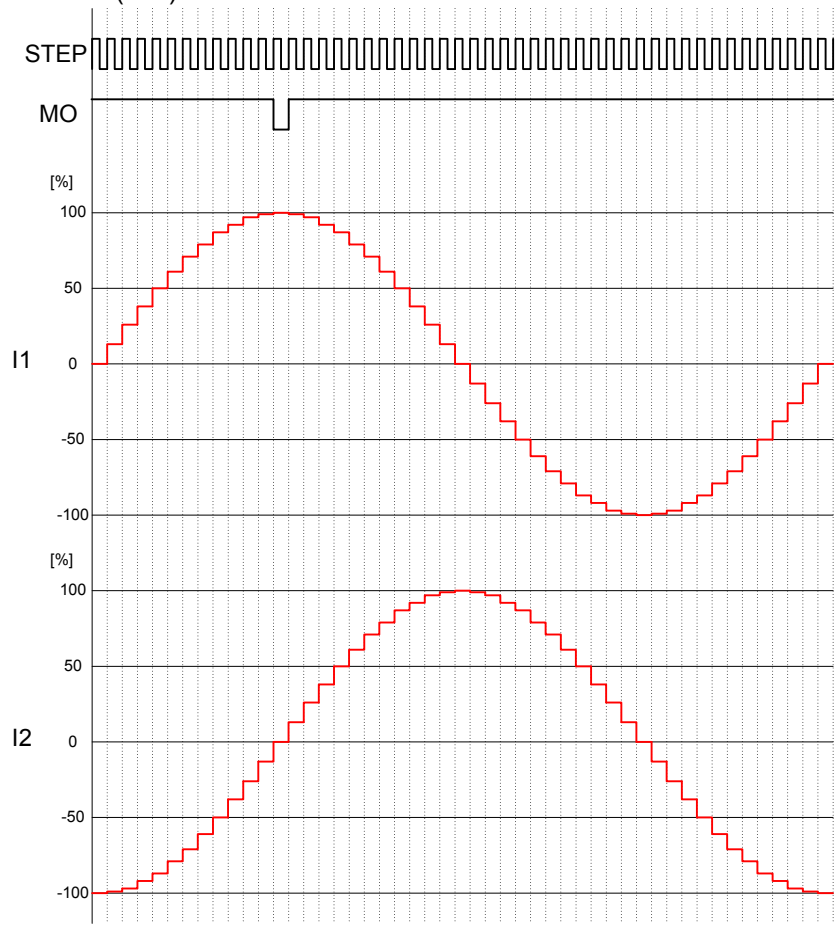
1/16 STEP (CW)



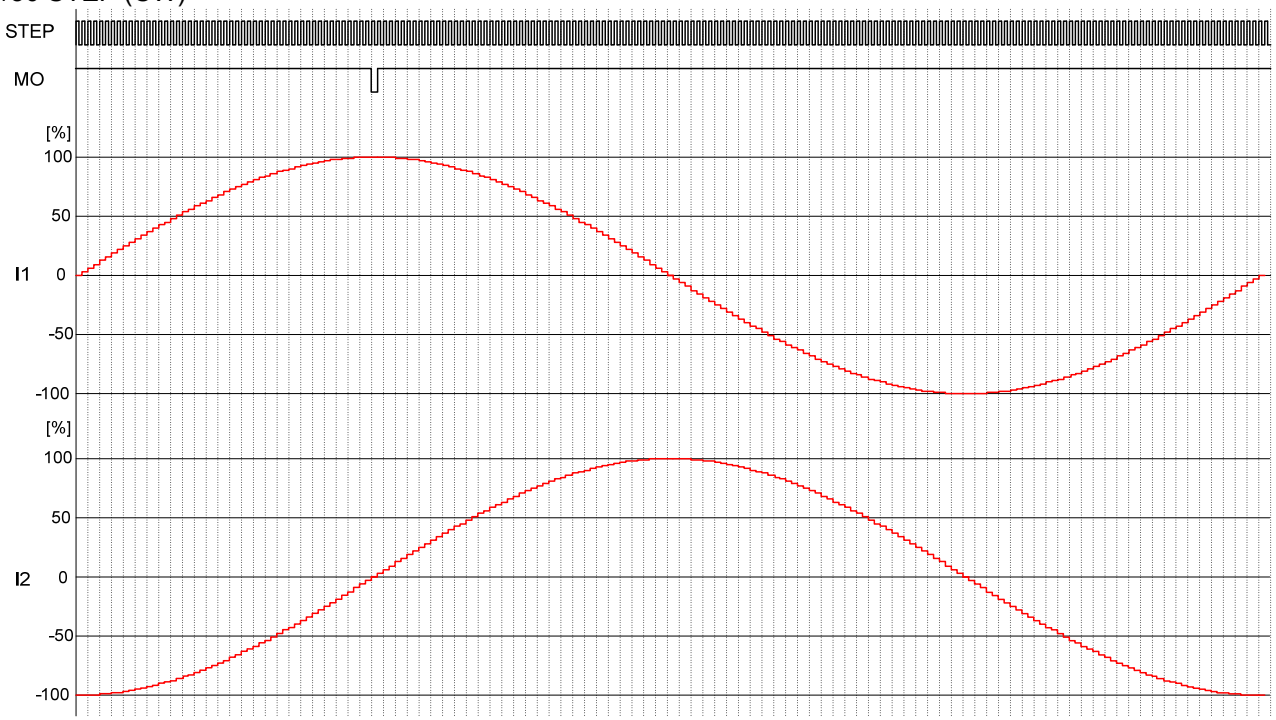
1/128 STEP (CW)



1/12 STEP (CW)



1/50 STEP (CW)

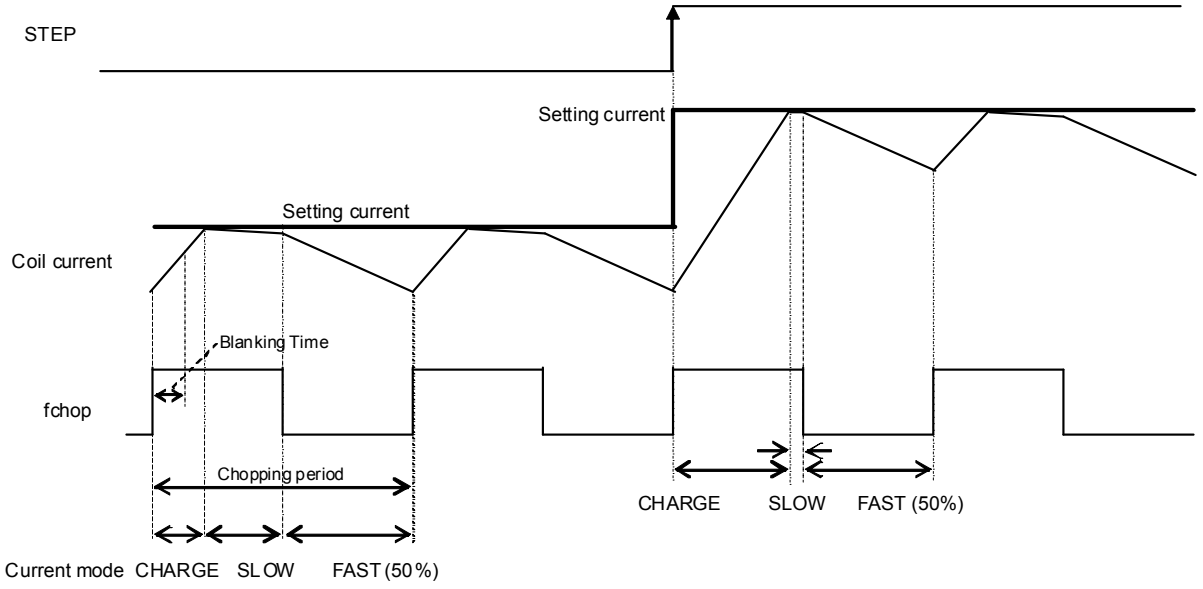


(2-19) Current control operation

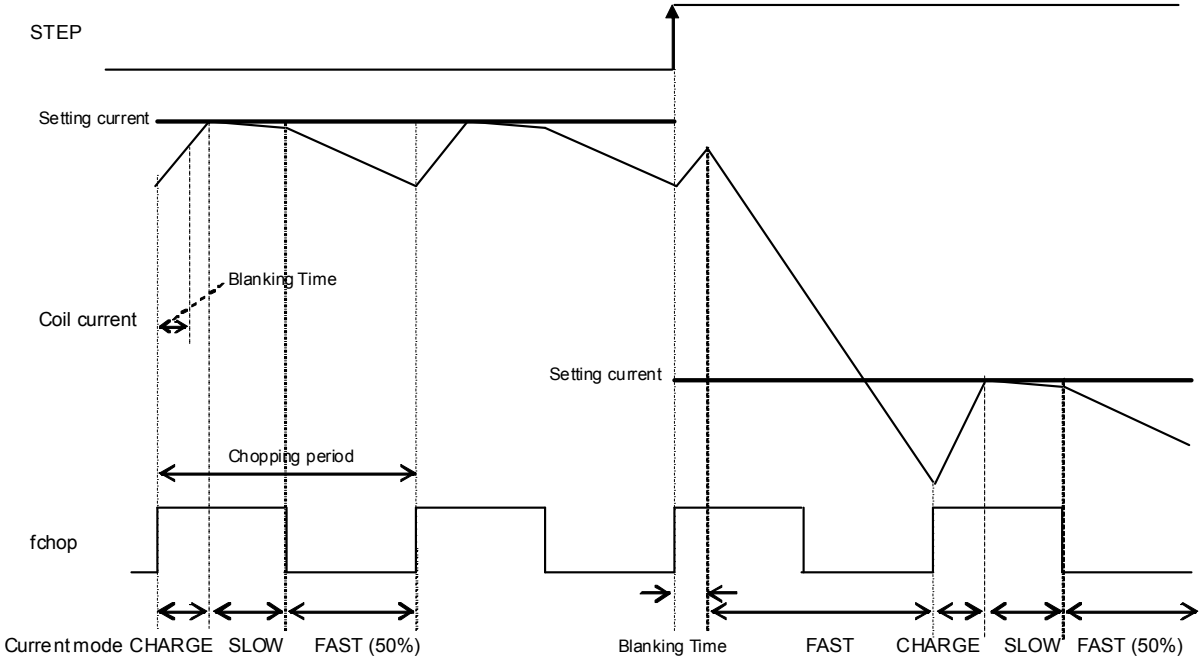
MIXED DECAY current control operation

MIXED DECAY current control operation can change 50%FAST mode and 25%FAST mode by serial data setting.

(Sine-wave increasing direction)



(Sine-wave increasing direction)



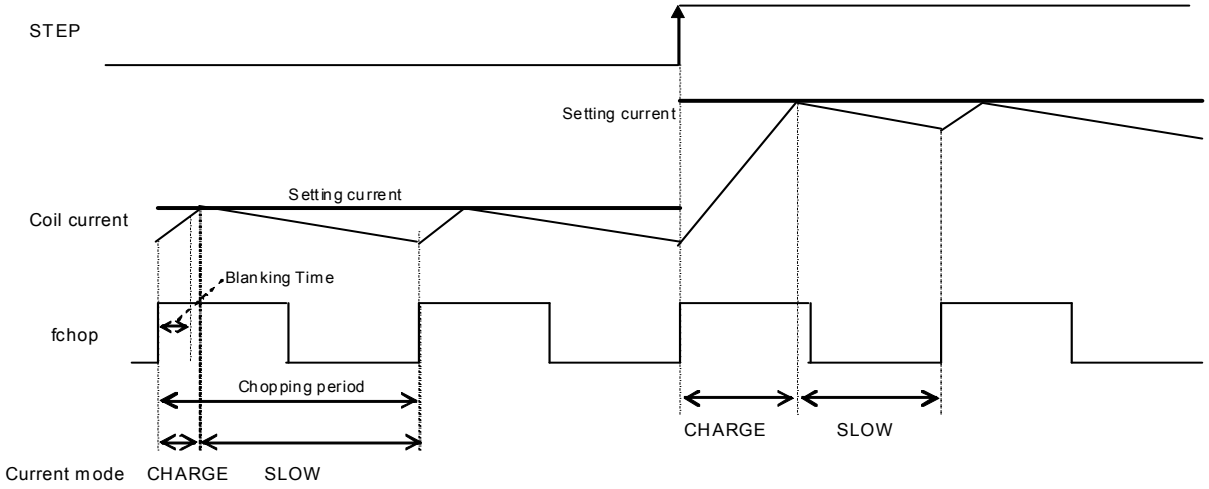
In each current mode, the operation sequence is as described below

- According to chopping (PWM) period, the CHARGE mode begins. In the time defined as the “blanking time” the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF).
- By the setting of the DECAY mode, as for the 50%FAST mode, 50% of the chopping (PWM) period become FAST_DECAY mode, and, as for the 25%FAST mode, 25% of the chopping (PWM) period become FAST_DECAY mode.

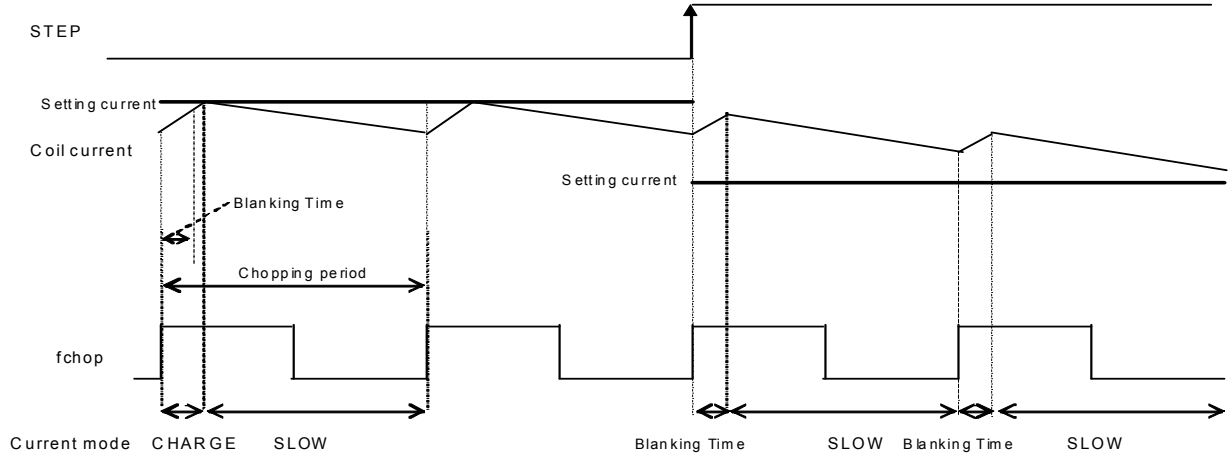
Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the Triangle wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

SLOW DECAY current control operation

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



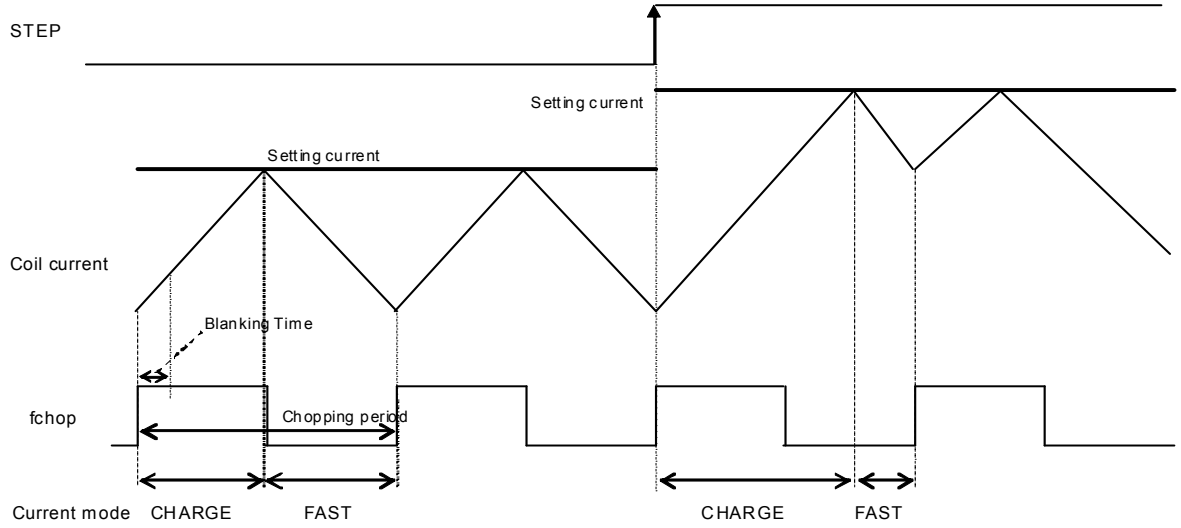
Each of current modes operates with the follow sequence.

- According to chopping (PWM) period, the CHARGE mode begins.
  A period of CHARGE mode (Blanking Time) is forcibly present, regardless of the current value of the coil current (ICOIL) and set current (IREF).
- After the period of the blanking time, the IC operates in CHARGE mode until ICOIL ≥ IREF. After that, the mode switches to the SLOW DECAY mode and the coil current is attenuated until the end of a chopping (PWM) period.

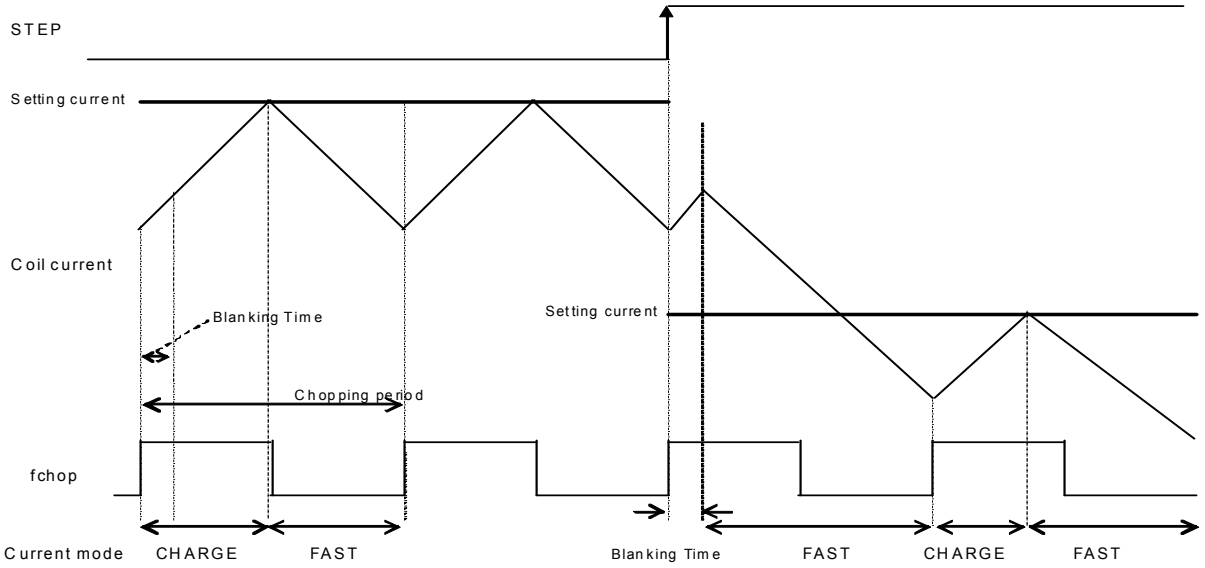
At the constant-current control in SLOW DECAY mode, following to the setting current from the coil current may take time (or not follow) for the current delay attenuation.

FAST DECAY current control operation

(Sine-wave increasing direction)



(Sine-wave increasing direction)

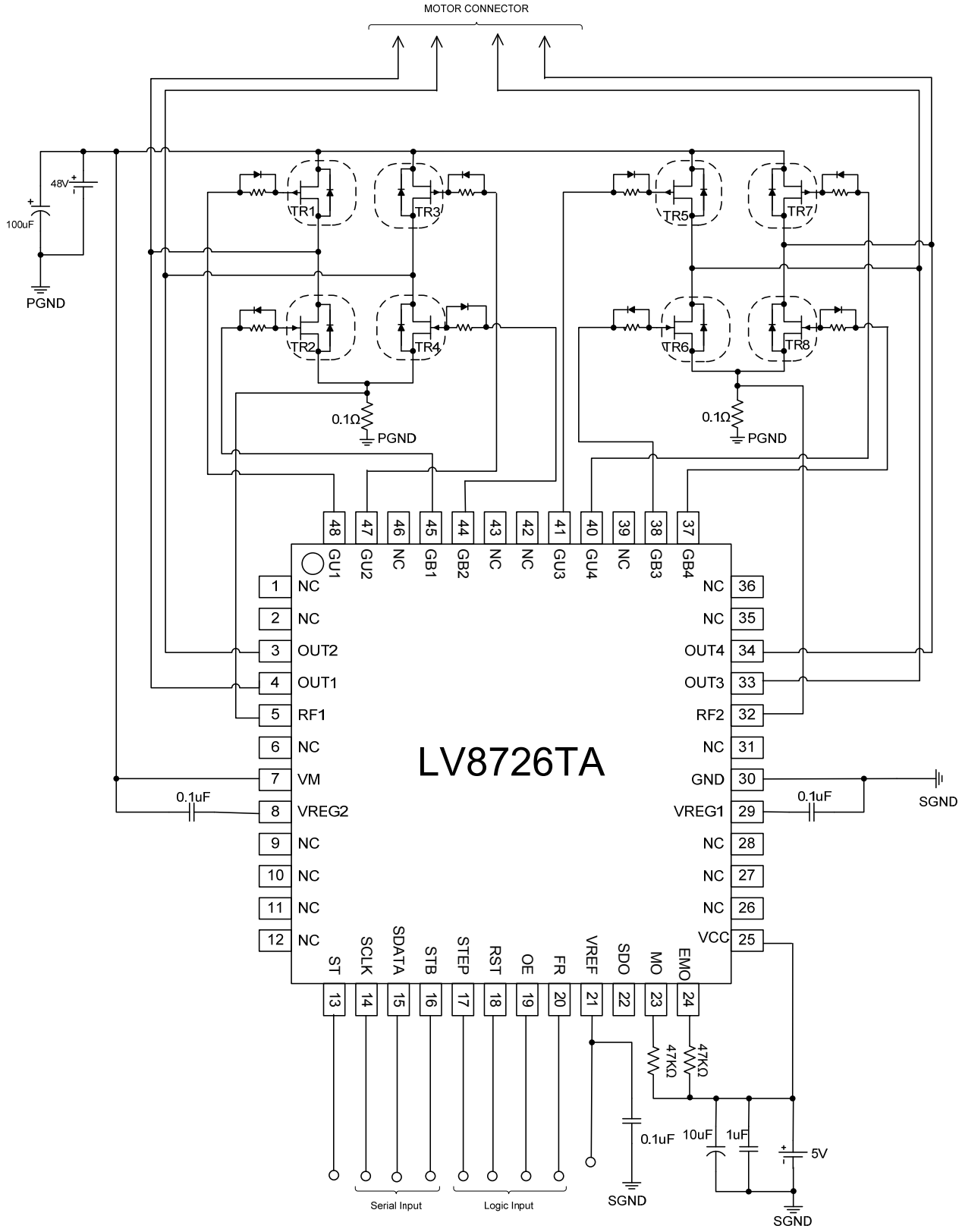


Each of current modes operates with the follow sequence.

- According to chopping (PWM) period, the CHARGE mode begins.
  A period of CHARGE mode (Blanking Time) is forcibly present, regardless of the current value of the coil current (ICOIL) and set current (IREF).
- After the period of the blanking time, The IC operates in CHARGE mode until ICOIL ≥ IREF. After that, the mode switches to the FAST DECAY mode and the coil current is attenuated until the end of a chopping (PWM) period.

At the constant-current control in FAST DECAY mode, following to the setting current from the coil current takes short-time for the current fast attenuation, but, the current ripple value may be higher.

Application Circuit Example



Setting of constant current

When VREF = 1.5V, RF= 0.1Ω

Iout = (VREF/5) / RF

= (1.5V/5) / 0.1Ω = 3.0A

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8726TA-NH	TQFP48 EP 7×7 (Pb-Free / Halogen Free)	1000 / Tape & Reel